WHAT IS CLAIMED IS:

1. A thin film transistor panel for a liquid crystal display comprising:

a substrate;

a plurality of data lines formed over the substrate and extending in a first direction;

a plurality of gate lines formed over the substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas, each of the plurality of pixel areas having a multi-bent band shape; and

a plurality of pixel electrodes each formed in a corresponding pixel area.

2. The thin film transistor panel of claim 1, wherein each of the plurality of data lines is curved periodically to form the multi-bent band shaped pixel areas.

3. The thin film transistor panel of claim 1, wherein each of the plurality of pixel electrodes comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion.

4. The thin film transistor panel of claim 2, wherein each of the plurality of data lines comprise a first set of oblique portions and a second set of oblique portions, the first set of oblique portions being angled counterclockwise by about 45° from the plurality of gate lines and the second set of oblique portions being angled clockwise by about 45° from the plurality of gate lines.

5. The thin film transistor panel of claim 1, further comprising:

a plurality of storage electrode lines formed over the substrate and extending substantially in the second direction.

6. The thin film transistor panel of claim 5, further comprising:

a plurality of sets of storage electrodes connected to each storage electrode line, each set of storage electrodes comprising a pair of first storage electrodes extending substantially in the first direction and a second storage electrode that connects the first storage electrodes; and

a plurality of connectors that connect the first storage electrodes in neighboring sets of storage electrodes.

7. The thin film transistor panel of claim 6, wherein each of the first storage electrodes is curved periodically.

8. The thin film transistor panel of claim 1, further comprising:

a gate insulating layer formed over the plurality of gate lines.

9. The thin film transistor panel of claim 8, further comprising:

a plurality of semiconductor stripes formed over the gate insulating layer and extending substantially in the first direction.

10. The thin film transistor panel of claim 9, wherein each gate line comprises a plurality of gate electrodes.

11. The thin film transistor panel of claim 10, wherein each semiconductor stripe comprises a plurality of projections, each projection extending towards a corresponding gate electrode.

12. The thin film transistor panel of claim 11, further comprising a plurality of ohmic contact stripes and islands formed over the plurality of semiconductor stripes.

13. The thin film transistor panel of claim 12, wherein each ohmic contact stripe comprises a plurality of projections, each of the projections of the contact stripes and the ohmic contact islands located in pairs over the projections of the semiconductor stripes.

14. The thin film transistor panel of claim 13, wherein the plurality of data lines are formed over the plurality of ohmic contact stripes.

15. The thin film transistor panel of claim 14, further comprising a plurality of drain electrodes each formed over a corresponding ohmic contact island.

16. The thin film transistor panel of claim 15, wherein each data line comprises a plurality of source electrodes, each source electrode extending towards a corresponding drain electrode so that each source electrode is separated and opposite from a corresponding drain electrode with respect to a corresponding gate electrode.

17. The thin film transistor panel of claim 16, further comprising:

a passivation layer formed over the plurality of data lines and the plurality of drain electrodes.

18. The thin film transistor panel of claim 17, wherein each data line comprises an expansion portion for electrical connection.

19. The thin film transistor panel of claim 18, wherein each gate line comprises an expansion portion for electrical connection

20. The thin film transistor panel of claim 19, wherein the plurality of data lines and the plurality of drain electrodes each comprise a lower film and an upper film.

21. The thin film transistor panel of claim 6, further comprising:

a gate insulating layer formed over the plurality of gate lines and a passivation layer formed over the plurality of data lines and the plurality of drain electrodes

and wherein one of the first storage electrodes in each pair of first storage electrodes has a free end portion and an end portion fixed to a corresponding storage electrode line, and another of the first storage electrodes in each pair of first storage electrodes has an end portion that is connected to the connector and an end portion that is fixed to a corresponding storage electrode line.

22. The thin film transistor panel of claim 17, wherein the passivation layer comprises a plurality of first contact holes exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes exposing the lower films of the expansions of the plurality of data lines.

23. The thin film transistor panel of claim 22, wherein the passivation layer and the gate insulating layer comprise a plurality of third contact holes exposing the expansions of the plurality of gate lines.

24. The thin film transistor panel of claim 23, wherein the plurality of first, second, third, fourth and fifth contact holes have stepped profiles.

25. The thin film transistor panel of claim 23, wherein the plurality of pixel electrodes are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes.

26. The thin film transistor panel of claim 21, wherein, the passivation layer and the gate insulating layer comprise a plurality of fourth contact holes exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end and a plurality of fifth contact holes exposing free end portions of the storage electrodes having a free end

and further comprising:

a plurality of storage connecting bridges formed over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes.

27. The thin film transistor panel of claim 15, wherein the plurality of semiconductor stripes have substantially the same planar shape as the plurality of data lines and the plurality of drain electrodes.

28. The thin film transistor panel of claim 17, wherein the passivation layer comprises a first passivation layer and a second passivation layer, and a plurality of color filters is formed between the first passivation layer and the second passivation layer.

29. The thin film transistor panel of claim 17, further comprising:

a plurality of color filters formed over the passivation layer, the plurality of pixel electrodes formed over the plurality of color filters.

30. A liquid crystal display comprising the thin film transistor panel of claim 1.

31. A liquid crystal display comprising:

a thin film transistor panel comprising:

a first substrate;

a plurality of data lines formed over the first substrate and extending in a first direction;

a plurality of gate lines formed over the first substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas, each of the plurality of pixel areas having a multi-bent band shape; and

a plurality of pixel electrodes each formed in a corresponding pixel area;

a common electrode panel, comprising:

a second substrate;

a black matrix formed over the second substrate; and

a common electrode formed over the black matrix; and

a liquid crystal layer formed between the thin film transistor panel and the common electrode panel.

32. The liquid crystal display of claim 30, wherein each of the plurality of pixel electrodes comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion.

33. The liquid crystal display of claim 31, further comprising:

a plurality of color filters formed over the black matrix and the second substrate.

34. A method of forming a thin film transistor panel of a liquid crystal display comprising:

forming a plurality of data lines over a substrate, the plurality of data lines extending in a first direction;

forming a plurality of gate lines over the substrate, the plurality of gate lines extending in a second direction and crossing the plurality of data lines to form a plurality of pixel areas, each of the plurality of pixel areas having a multi-bent band shape; and

forming a pixel electrode in each of the plurality of pixel areas.

35. The method of claim 34, wherein the step of forming a plurality of data lines comprises forming each of the plurality of data lines with a periodically curved shape.

36. The method of claim 34, wherein the step of forming the plurality of pixel electrodes comprises forming each pixel electrode with a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion.

37. The method of claim 35, wherein the step of forming a plurality of data lines comprises forming each of the plurality of data lines with a first set of oblique portions and a second set of oblique portions, the first set of oblique portions being angled counterclockwise by about 45° from the plurality of gate lines and the second set of oblique portions being angled clockwise by about 45° from the plurality of gate lines.

38. The method of claim 34, further comprising:

forming a plurality of storage electrode lines over the substrate and extending substantially in the second direction.

39. The thin film transistor panel of claim 38, further comprising:

forming a plurality of sets of storage electrodes connected to each storage electrode line, each set of storage electrodes comprising a pair of first storage electrodes extending substantially in the first direction and a second storage electrode that connects the first storage electrodes; and

forming a plurality of connectors that connect the first storage electrodes in neighboring sets of storage electrodes.

40. The method of claim 39, wherein the step of forming a plurality of gate lines and the step of forming a plurality of storage electrode lines are performed simultaneously by depositing a first lower conductive film and a first upper conductive film on the substrate and etching the first lower conductive film and the first upper conductive film.

41. The method of claim 40, further comprising:

forming a gate insulating layer over the plurality of gate lines and the plurality of storage electrode lines.

42. The method of claim 41, further comprising:

forming a plurality of semiconductor stripes over the gate insulating layer and extending substantially in the first direction.

43. The method of claim 42, wherein the step of forming a plurality of gate lines comprises forming each gate line with a plurality of gate electrodes.

44. The method of claim 43, wherein the step of forming a plurality of semiconductor stripes comprises forming each semiconductor stripe with a plurality of projections, each projection extending towards a corresponding gate electrode.

45. The method of claim 44, wherein the step of forming a plurality of semiconductor stripes comprises forming an intrinsic semiconductor layer and an extrinsic semiconductor layer over the gate insulating layer, and etching the intrinsic semiconductor layer and the extrinsic semiconductor layer to form a plurality of intrinsic semiconductor stripes and a plurality of extrinsic semiconductor stripes, the plurality of intrinsic semiconductor stripes forming the plurality of semiconductor stripes.

46. The method of claim 45, further comprising:

depositing a second lower conductive film and a second upper conductive film over the plurality of intrinsic semiconductor stripes and the plurality of extrinsic semiconductor stripes; and

patterning the second lower conductive film and the second upper conductive film to form the plurality of data lines and a plurality of drain electrodes, each of the plurality of data lines comprising a plurality of source electrodes.

47. The method of claim 46, further comprising:

removing portions of the extrinsic semiconductor stripes that are not covered with the plurality of data lines and the drain electrodes to form a plurality of ohmic contact stripes and islands, each of the plurality of ohmic contact stripes comprising a plurality of projections, each of the projections of the contact stripes and the ohmic contact islands located in pairs over the projections of the semiconductor stripes.

48. The method of claim 47, further comprising:

forming a passivation layer over the plurality of data lines and the plurality of drain electrodes.

49. The method of claim 48, wherein the step of forming a plurality of data lines comprises forming each data line with an expansion portion for electrical connection.

50. The method of claim 49, wherein the step of forming a plurality of gate lines comprises forming each gate line with an expansion portion for electrical connection.

51. The method of claim 50, wherein the step of forming a plurality of sets of storage electrodes comprises forming one of the first storage electrodes in each pair of first storage electrodes with a free end portion and an end portion fixed to a corresponding storage electrode line, and another of the first storage electrodes in each pair of first storage electrodes with an end portion that is connected to the connector and an end portion that is fixed to a corresponding storage electrode line.

52. The method of claim 51, further comprising:

forming a plurality of first contact holes in the passivation layer that expose the lower films of the plurality of drain electrodes and a plurality of second contact holes in the passivation layer that expose the lower films of the expansions of the plurality of data lines.

53. The method of claim 52, further comprising:

forming a plurality of third contact holes in the passivation layer and the gate insulating layer exposing the expansions of the plurality of gate lines, a plurality of fourth contact holes in the passivation layer and the gate insulating layer exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end, and forming a plurality of fifth contact holes in the passivation layer and the gate insulating layer exposing free end portions of the storage electrodes having a free end.

54. The method of claim 53, wherein the step of forming the plurality of first, second, third, fourth and fifth contact holes comprises forming the plurality of first, second, third, fourth and fifth contact holes with stepped profiles.

55. The method of claim 54, wherein the step of forming the plurality of first, second, third, fourth and fifth contact holes comprises:

exposing the passivation layer through a photo-mask having a plurality of transmissive areas and a plurality of slit areas disposed around the transmissive areas.

56. The method of claim 51, wherein the plurality of pixel electrodes are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes.

57. The method of claim 52, further comprising:

forming a plurality of storage connecting bridges over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes.